RTX-02D SINGLE 8255 CARD

1. INTRODUCTION

THE RTX-02D SINGLE 8255 CARD IS A PROGRAMABLE INPUT/OUTPUT INTER-FACE FOR IBM PC/XT/AT OR COMPATIBLE COMPUTER. THIS CARD CONTAINS 24 I/O LINE, ALL MODES OF OPERATION ARE SOFTWARE PROGRAMABLE.
THE BOARD'S BASE I/O ADDRESS IS JUMPER SELECTABLE TO ONE OF EIGHT I/O LOCATION. ALL EXTERNAL I/O WITH THE RTX-02D IS DONE THROUGH A 25-PIN FEMALE CONNECTOR. THAT IS ACCESSIBLE THROUGH THE REAR PANEL OF THE COMPUTER AFTER THE BOARD IS INSTALLED.

2. INSTALLATION

BASE ADDRESS SELECTION (JP1) : &H200 – &H203
&H240 – &H243
&H280 – &H283
&H2C0 – &H2C3
&H300 – &H303
&H340 – &H343
&H380 – &H383
&H3C0 – &H3C3

RTX-02D SYSTEM BOARD DEFAULT &H200 – &H203

&H200 – PORT A READ WRITE BUFFER
&H201 – PORT B READ WRITE BUFFER
&H202 – PORT C READ WRITE BUFFER
&H203 – 8255 CONTROL REGISTER

3. RTX-02D DEMO PROGRAM LIST

```
100 REM * RTX-02D SINGLE 8255 CARD DEMO PROGRAM *
110 SCREEN 0,0,0: WIDTH 80,25: KEY OFF: CLS
120 PORT = &H200
130 OUT PORT+3, &H80
140 A=0
150 FOR I=0 TO 2
160 OUT PORT+I, A
170 NEXT I
180 FOR DELAY=0 TO 1000: NEXT DELAY
190 A=&HFF
200 FOR I=0 TO 2
210 OUT PORT+I, A
220 NEXT I
230 GOTO 120
```

4. I/O CONNECTOR

P1 PIN ASSIGNMENTS

1	PA0	14	PB5
2	PA1	15	PB6
3	PA2	16	PB7
4	PA3	17	PC0
5	PA4	18	PC1
6	PA5	19	PC2
7	PA6	20	PC3
8	PA7	21	PC4
9	PB0	22	PC5
10	PB1	23	PC6
11	PB2	24	PC7
12	PB3	25	GND
13	PB4		

APPENDIX A μPD8255A-2 μPD8255A-5

PROGRAMMABLE PERIPHERAL INTERFACES

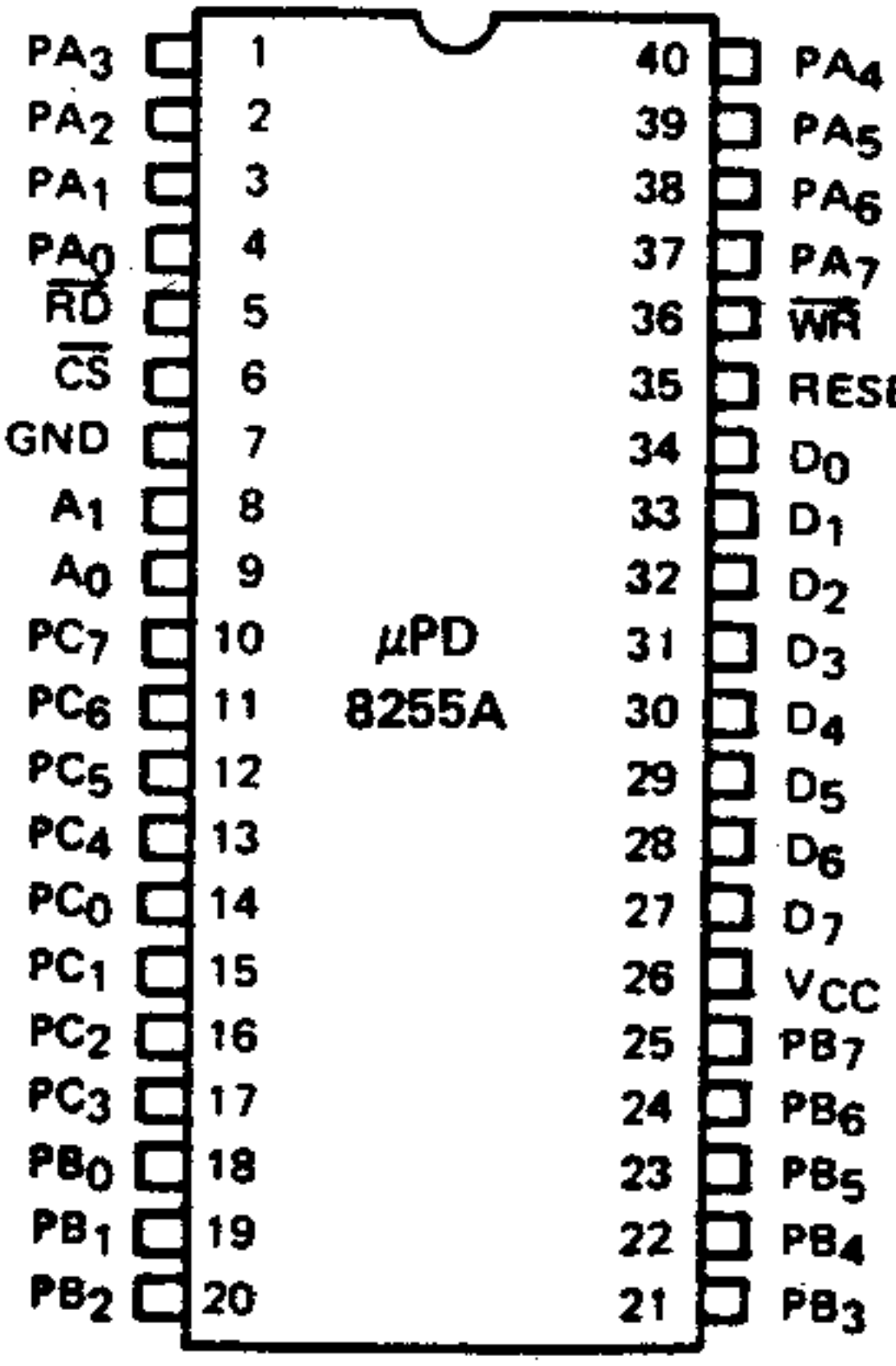
DESCRIPTION

THE μPD8255A IS A GENERAL PURPOSE PROGRAMMABLE INPUT/OUTPUT DEVICE DESIGNED FOR USE WITH THE 8080A/8085A MICROPROCESSORS. TWENTY-FOUR (24) I/O LINES MAY BE PROGRAMMED IN TWO GROUPS OF TWELVE (GROUP I AND GROUP II) AND USED IN THREE MODES OF OPERATION. IN THE BASIC MODE, (MODE 0), EACH GROUP OF TWELVE I/O PINS MAY BE PROGRAMMED IN SETS OF 4 TO BE INPUT OR OUTPUT. IN THE STROBED MODE, (MODE 1), EACH GROUP MAY BE PROGRAMMED TO HAVE 8 LINES OF INPUT OR OUTPUT. THREE OF THE REMAINING FOUR PINS IN EACH GROUP ARE USED FOR HANDSHAKING STROBES AND INTERRUPT CONTROL SIGNALS. THE BI-DIRECTIONAL BUS MODE, (MODE 2), USES THE 8 LINES OF PORT A FOR A BI-DIRECTIONAL BUS, AND FIVE LINES FROM PORT C FOR BUS CONTROL SIGNALS. THE μPD8255A IS PACKAGE IN 40-PIN PLASTIC DUAL-IN-LINE PACKAGES.

FEATURES

- FULL COMPATIBLE WITH THE 8080A/8085 MICROPROCESSOR FAMILIES
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE
- 24 PROGRAMMABLE I/O PINS
- DIRECT BIT SET/RESET EASES CONTROL APPLICATION INTERFACES
- 8 – 4 mA DARLINGTON DRIVE OUTPUTS FOR PRINTERS AND DISPLAYS.
- LSI DRASTICALLY REDUCES SYSTEM PACKAGE COUNT
- STANDARD 40-PIN DUAL-IN-LINE PLASTIC.

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

APPENDIX B μPD8255A

FUNCTIONAL DESCRIPTION

GENERAL

THE μPD8255A PROGRAMMABLE PERIPHERAL INTERFACE (PPI) IS DESIGNED FOR USE IN 8080A/8085A MICROPROCESSOR SYSTEMS. PERIPHERAL EQUIPMENT CAN BE EFFECTIVELY AND EFFICIENTLY INTERFACED TO THE 8080A/8085A DATA AND CONTROL BUSSES WITH THE μPD8255A. THE μPD8255A IS FUNCTIONALLY CONFIGURED TO BE PROGRAMMED BY SYSTEM SOFTWARE TO AVOID EXTERNAL LOGIC FOR PERIPHERAL INTERFACES.

DATA BUS BUFFER

THE 3-STATE, BIDIRECTIONAL, 8-BIT DATA BUS BUFFER (D_0-D_7) OF THE μPD8255A CAN BE DIRECTLY INTERFACED TO THE PROCESSOR'S SYSTEM DATA BUS (D_0-D_7). THE DATA BUS BUFFER IS CONTROLLED BY EXECUTION OF IN AND OUT INSTRUCTIONS BY THE PROCESSOR. CONTROL WORLDS AND STATUS INFORMATION ARE ALSO TRANSMITTED VIA THE DATA BUS BUFFER.

READ/WRITE AND CONTROL LOGIC

THIS BLOCK MANAGES ALL OF THE INTERNAL AND EXTERNAL TRANSFERS OF DATA, CONTROL AND STATUS. THROUGH THIS BLOCK, THE PROCESSOR ADDRESS AND CONTROL BUSSES CAN CONTROL THE PERIPHERAL INTERFACES.

CHIP SELECT, $\overline{CS}$, PIN 6

A LOGIC LOW, V_{IL}, ON THIS INPUT ENABLES THE μPD8255A FOR COMMUNICATION WITH THE 8080A/8085A.

READ, $\overline{RD}$, PIN 5

A LOGIC LOW, V_{IL}, ON THIS INPUT ENABLES THE μPD8255A TO SEND DATA OR STATUS TO THE PROCESSOR VIA THE DATA BUS BUFFER.

WRITE, $\overline{WR}$, PIN 36

A LOGIC LOW V_{IL}, ON THIS INPUT ENABLES THE DATA BUS BUFFER TO RECEIVE DATA OR CONTROL WORDS FROM THE PROCESSOR.

PORT SELECT 0, A_0, PIN 9

PORT SELECT 1, A_1, PIN 8

THESE TWO INPUTS ARE USED IN CONJUNCTION WITH $\overline{CS}$, $\overline{RD}$, AND $\overline{WR}$ TO CONTROL THE SELECTION OF ONE OF THREE PORTS ON THE CONTROL WORD REGISTER. A_0 AND A_1 ARE USUALLY CONNECTED TO A_0 AND A OF THE PROCESSOR ADDRESS BUS.

RESET PIN 35

A LOGIC HIGH, V_{IH}, ON THIS INPUT CLEARS THE CONTROL REGISTER AND SETS PORTS, A, B, AND C TO THE INPUT MODE. THE INPUT LATCHES IN PORTS A, B, AND C ARE NOT CLEARED.

GROUP I AND GROUP II CONTROLS

THROUGH AN OUT INSTRUCTION IN SYSTEM SOFTWARE FROM THE PROCESSOR, A CONTROL WORD IS TRANSMITTED TO THE μPD8255A. INFORMATION SUCH AS "MODE," "BIT SET," AND "BIT RESET" IS USED TO INITIALIZE THE FUNCTIONAL CONFIGURATION OF EACH I/O PORT.

EACH GROUP (I AND II) ACCEPTS "COMMANDS" FROM THE READ/WRITE CONTROL LOGIC AND "CONTROL WORDS" FROM THE INTERNAL DATA BUS AND IN TURN CONTROLS ITS ASSOCIATED I/O PORT.

EACH GROUP (I AND II) ACCEPTS "COMMANDS" FROM THE READ/WRITE CONTROL LOGIC AND "CONTROL WORDS" FROM THE INTERNAL DATA BUS AND IN TURN CONTROLS ITS ASSOCIATED I/O PORTS.

GROUP I – PORT A AND UPPER PORT C (PC_7-PC_4)

GROUP II – PORT B AND LOWER PORT C (PC_3-PC_0)

WHILE THE CONTROL WORLD REGISTER CAN BE WRITTEN INTO, THE CONTENTS CANNOT TO READ BACK TO THE PROCESSOR.

PORTS A, B, AND C

THE THREE 8-BIT I/O PORTS (A, B, AND C) IN THE μPD8255A CAN ALL BE CONFIGURED TO MEET A WIDE VARIETY OF FUNCTIONAL REQUIREMENTS THROUGH SYSTEM SOFTWARE. THE EFFECTIVENESS AND FLEXIBILITY OF THE μPD8255A ARE FURTHER ENHANCED BY SPECIAL FEATURES UNIQUE TO EACH OF THE PORTS.

PORT A = AN 8-BIT DATA OUTPUT LATCH/BUFFER AND DATA INPUT LATCH.

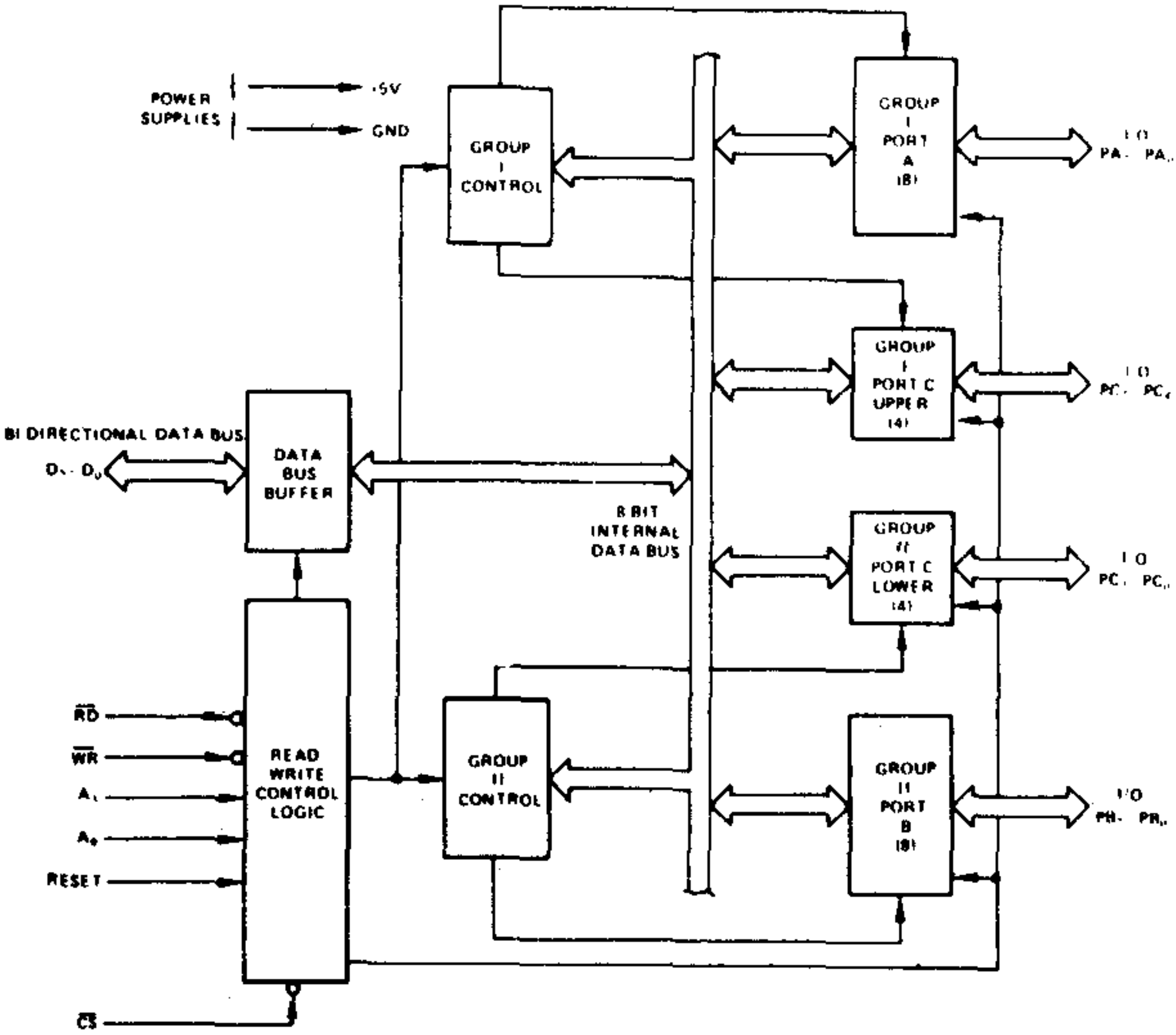
PORT B = 8-BIT DATA INPUT/OUTPUT LATCH/BUFFER AND AN 8-BIT DATA INPUT BUFFER.

PORT C = AN 8-BIT OUTPUT LATCH/BUFFER AND A DATA INPUT BUFFER (INPUT NOT LATCHED)

PORT C MAY BE DIVIDED INTO TWO INDEPENDENT 4-BIT CONTROL AND STATUS PORTS FOR USE WITH PORTS A AND B.

APPENDIX C μPD8255A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

OPERATING TEMPERATURE ..... 0°C TO +70°C

STORAGE TEMPERATURE ..... −65°C TO +150°C

VOLTAGE ON ANY PIN WITH RESPECT TO V_{SS} ..... −0.5 TO +7 VOLTS

NOTE: ① WITH RESPECT TO V_{SS}

T_a = 25°C

*COMMENT: STRESS ABOVE THOSE LISTED UNDER "ABSOLUTE MAXIMUM RATINGS" MAY CAUSE PERMANENT DAMAGE TO THE DEVICE. THIS IS STRESS RATING ONLY AND FUNCTIONAL OPERATION OF THE DEVICE AT THESE OR ANY OTHER CONDITIONS ABOVE THOSE INDICATED IN THE OPERATIONAL SECTIONS OF THIS SPECIFICATION IS NOT IMPLIED. EXPOSURE TO ABSOLUTE MAXIMUM RATING CONDITIONS FOR EXTENDED PERIODS MAY AFFECT DEVICE RELIABILITY.

DC CHARACTERISTICS

$T_a = 0°C$ TO $+70°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS μPD8255A MIN	LIMITS μPD8255A MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	V	
Input High Voltage	V_{IH}	2	V_{CC}	V	
Output Low Voltage	V_{OL}		0.45	V	(2)
Output High Voltage	V_{OH}	2.4		V	(3)
Darlington Drive Current	I_{OH} (1)	-1	-4	mA	V_{EXT} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}		10	μA	$V_{IN} = V_{CC}$
Input Leakage Current	I_{LIL}		-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}		±10	μA	$V_{OUT} = V_{CC}$: $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}		-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

NOTES: ① ANY SET OF EIGHT (8) OUTPUTS FROM EITHER PORT A,B, OR C CAN SOURCE 4 mA IR TO 1.5V.

② IOL = 2.5 mA FOR DB PORT; 1.7mA FOR PARIPHERAI

③ IOH = −400μA FOR dB PORT; −200 μA FOR PERIPHERAL PORTS

CAPACITANCE

$T_a = 25°C$; $V_{CC} = V_{SS} = 0V$

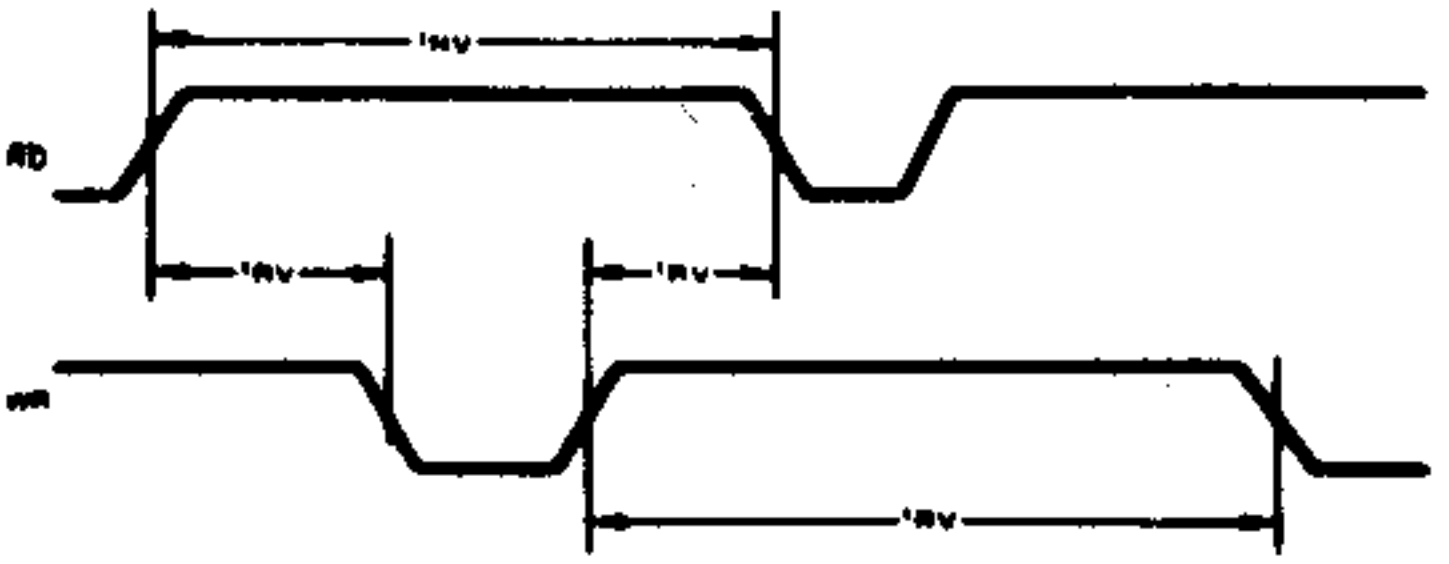
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

AC CHARACTERISTICS

$T_a = 0°C$ TO $+70°C$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	8255A-2 LIMITS		8255A-5 LIMITS		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Stable Before $\overline{READ}$	t_{AR}	0		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	200		250		ns	
Data Valid From $\overline{READ}$	t_{RD}		140		170	ns	$C_L = 150$ pF
Data Float After $\overline{READ}$	t_{DF}	10	100	10	100	ns ns	$C_L = 100$ pF $C_L = 15$ pF
Time Between $\overline{READS}$ and $\overline{WRITES}$	t_{RV}	200		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	200		250		ns	
Data Valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	0		0		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		350		350	ns	$C_L = 150$ pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	300		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		350		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	0		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		150		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		300		300	ns	$C_L = 150$ pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	250	20	250	ns	$C_L = 50$ pF $C_L = 15$ pF
$\overline{WR}$ = 1 To OBF = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To OBF = 1	t_{AOB}		350		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		300		300	ns	
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		300		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		400		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		300		300	ns	$C_L = 150$ pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		350		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		450		850	ns	$C_L = 150$ pF ③

NOTE: ① PERIOD OF RESET PULSE MUST BE AT LEAST 50 μS DURING OR AFTER POWER ON. SUBSEQUENT RESET PULSE CAN BE 500 NS MIN

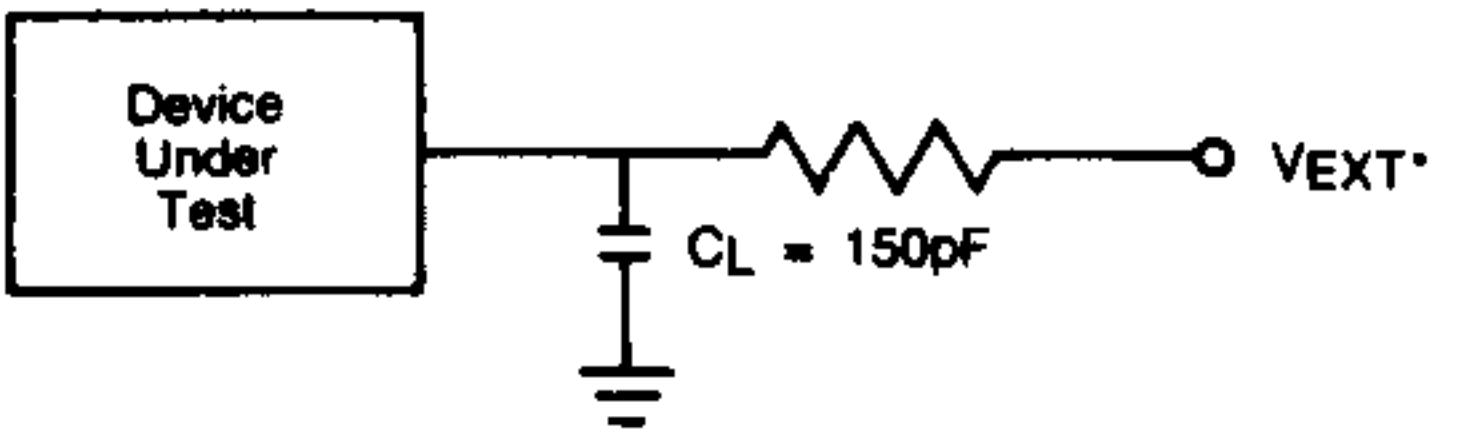


③ INTR ↑ MAY OCCUR AS EARLY AS $\overline{WR}$↓

AC TESTING INPUT, OUTPUT WAVEFORM

AC TESTING; INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 AND 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR a LOGIC 1 AND 0.8V FOR A LOGIC 0,

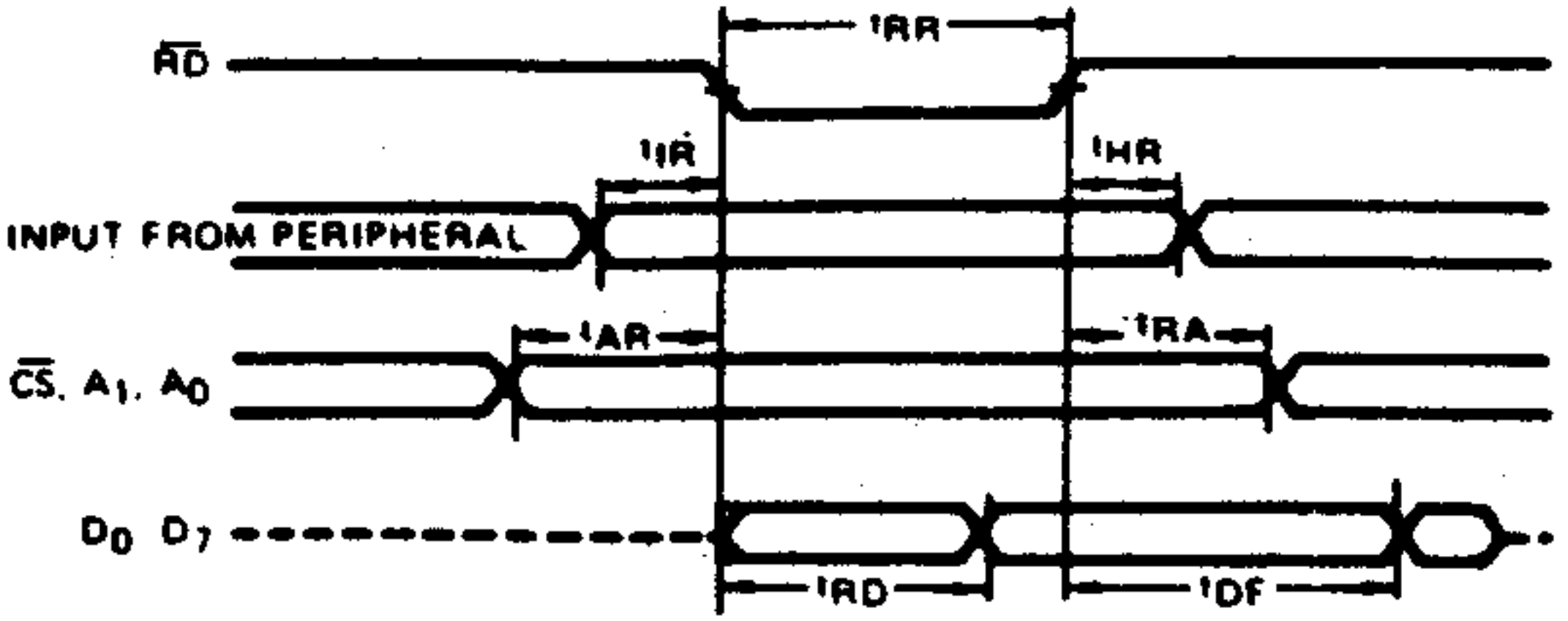
AC TESTING LOAD CIRCUIT



VEXT IS SET AT VARIOUS VOLTAGE DURING TESTING TO QUARANTEE THE SPECITICATION.

TIMING WAVEFORMS

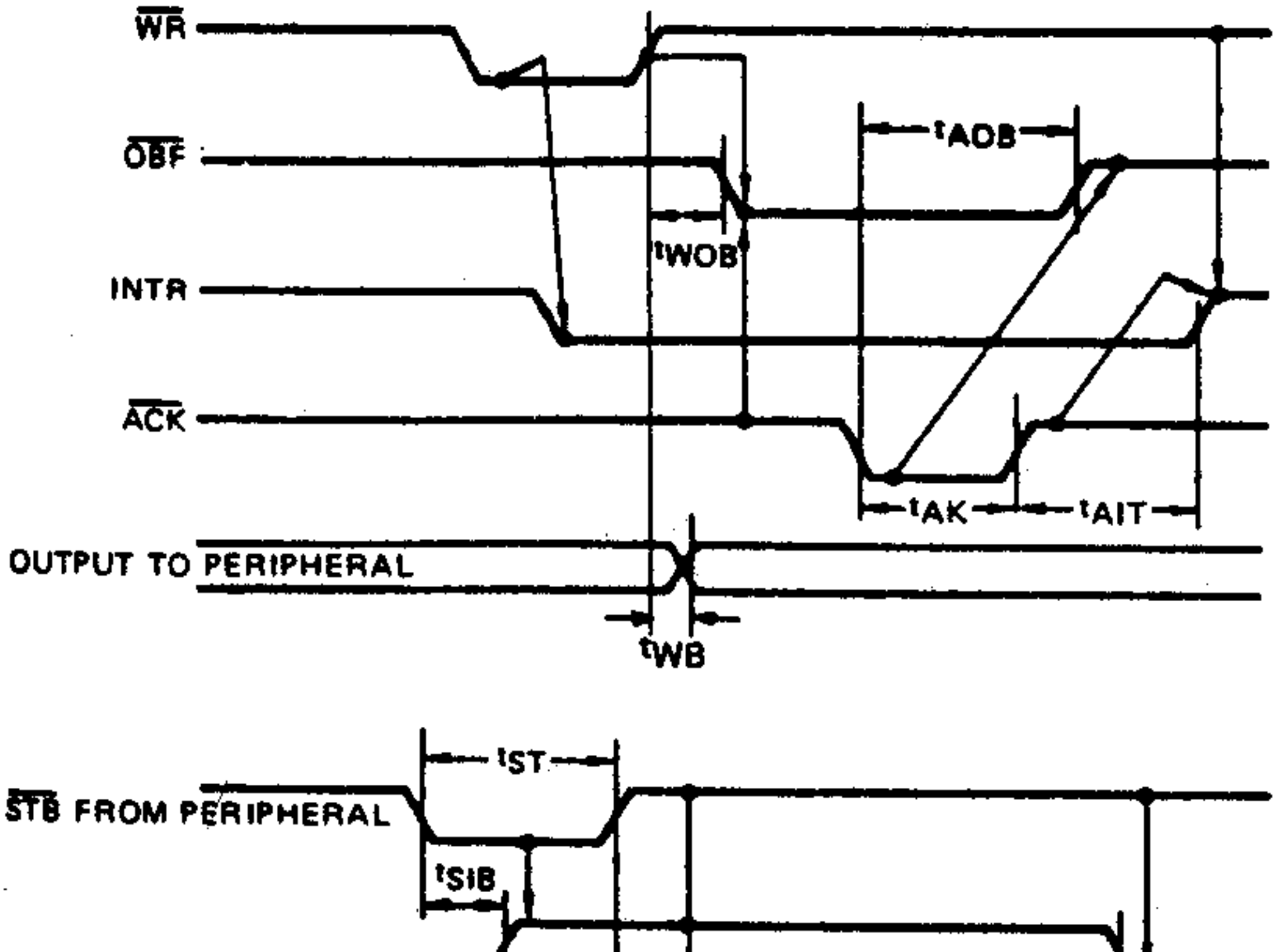
MODE 0



BASIC INPUT (READ)

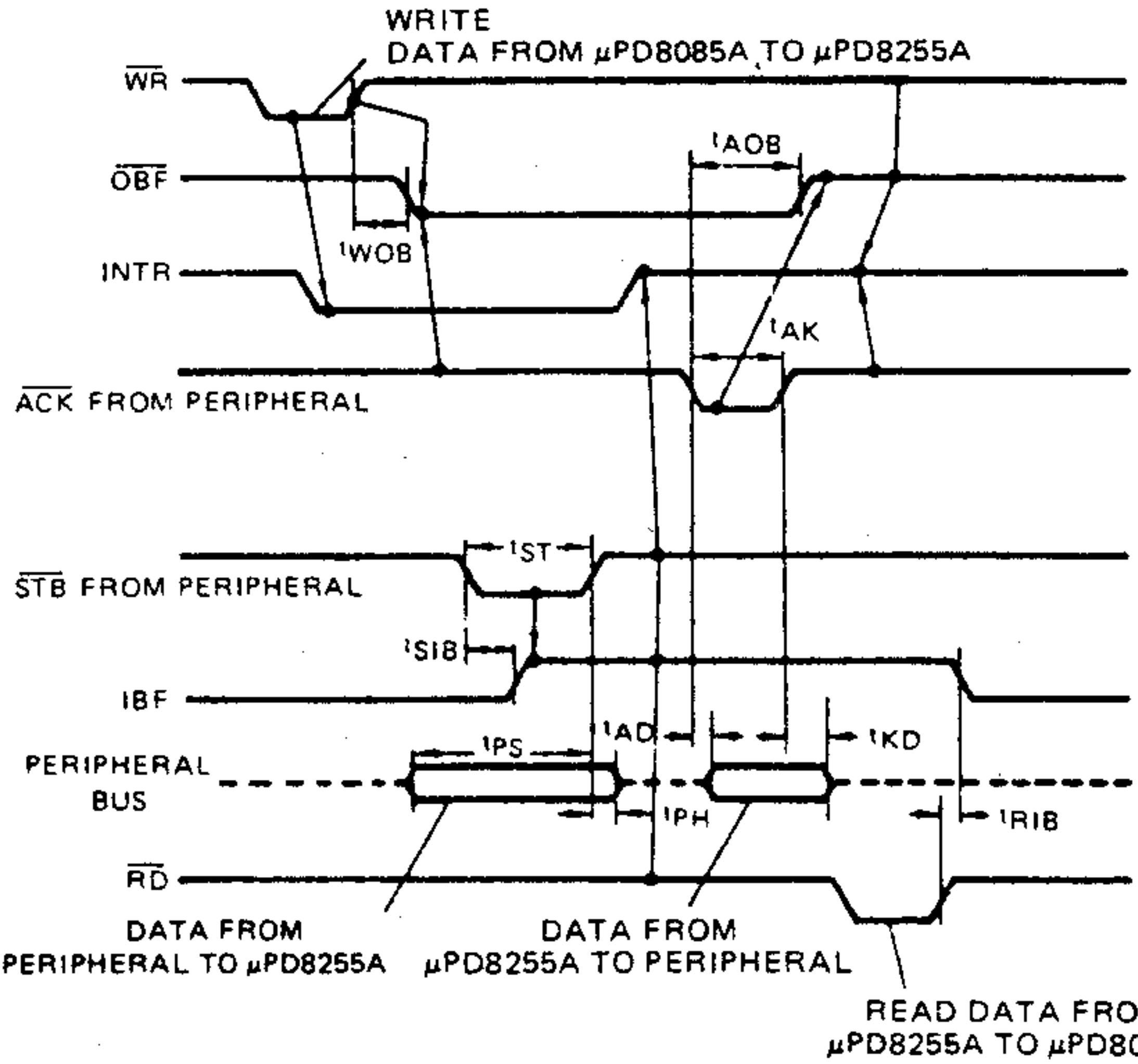
BASIC OUTPUT (WRITE)

MODE 1


WR
OBF
INTR
ACK
OUTPUT TO PERIPHERAL
tAOB
tWOB
tAK
tAIT
tWB
STB FROM PERIPHERAL
tST
tSIB
IBF
tSIT
INTR
tRIB
tRIT
RD
tPH
INPUT FROM PERIPHERAL
tPS

TIMING WAVEFORMS (CONT.)

MODE2



NOTE: ① ANY SEQUENCE WHERE $\overline{WR}$ OCCURS BEFORE $\overline{ACK}$ AND $\overline{STB}$ OCCURS BEFORE $\overline{RD}$ IS PERMISSIBLE.
(INTR = 1 BF, $\overline{MASK} \times \overline{STB} \times \overline{RD} + \overline{OBF} \times \overline{MASK} \times \overline{ACK} \times \overline{WR}$)

② WHEN THE μPD 8255A IS SET TO MODE 1 OR 2, $\overline{OBF}$ IS RESET TO BE HIGH (LOGIC 1).

THE μPD8255A CAN BE OPERATED IN MODES (0, 1 OR 2) WHICH ARE SELECTED BY APPROPRIATE CONTROL WORDS AND ARE DETAILED BELOW.

MODE 0

MODE 0 PROVIDES FOR BASIC INPUT AND OUTPUT OPERATIONS THROUGH EACH OF THE PORTS A, B, AND C. OUTPUT DATA IS LATCHED AND INPUT DATA FOLLOWS THE PERIPHERAL. NO "HAND-SHAKING" STROBES ARE NEEDED.

16 DIFFERENT CONFIGURATIONS IN MODE 0

TWO 8-BIT PORTS AND TWO 4-BIT PORTS

INPUT ARE NOT LATCHED OUTPUTS ARE LATCHED

MODE 1

MODE 1 PROVIDES FOR STROBED INPUT AND OUTPUT OPERATIONS WITH DATA TRANSFERRED THROUGH PORT A OR B AND HANDSHAKING THROUGH PORT C.

TWO I/O GROUPS (I AND II)

BOTH GROUPS CONTAIN AN 8-BIT DATA PORT AND A 4-BIT CONTROL/DATA PORT

BOTH 8-BIT DATA PORTS CAN BE EITHER LATCHED INPUT OR LATCHED OUTPUT

MODE 2

MODE 2 PROVIDES FOR STROBED BIDIRECTIONAL OPERATION USING PA_{0-7} AS THE BIDRECTIONAL LATCHED DATA BUS. PC_{3-7} IS USED FOR INTERRUPTS AND "HANDSHAK" BUS FLOW CONTROLS SIMILAR TO MODE 1. NOTE THAT PB_{0-7} AND PC_{0-2} MAY BE DEFINED AS MODE 0 OR 1, INPUT OR OUTPUT IN CONJUNCTION WITH PORT A IN MODE 2.

AN 8-BIT LATCHED BIDIRECTIONAL BUS PORT (PA_{0-7}) AND A 5-BIT CONTROL PORT (PC_{3-7})

BOTH INPUTS AND OUTPUTS ARE LATCHED

AN ADDITIONAL 8-BIT INPUT OR OUTPUT PORT WITH A 3-BIT CONTROL PORT

APPENDIX G μPD8255A

BASIC OPERATION

INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

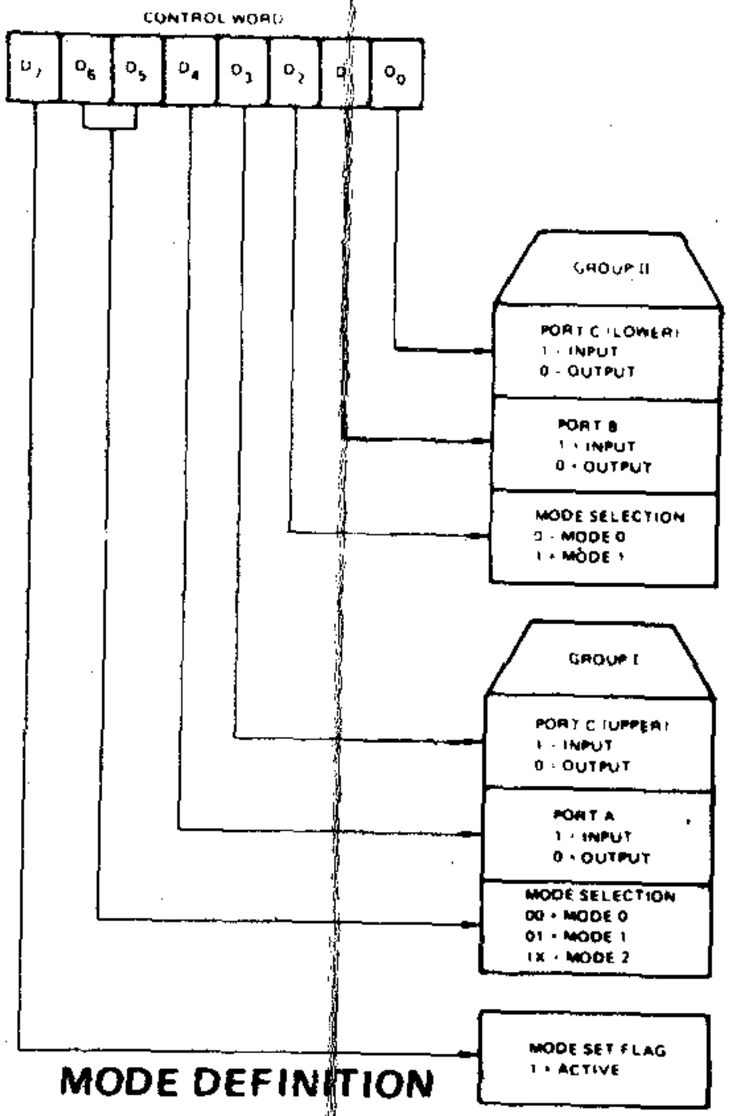
OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

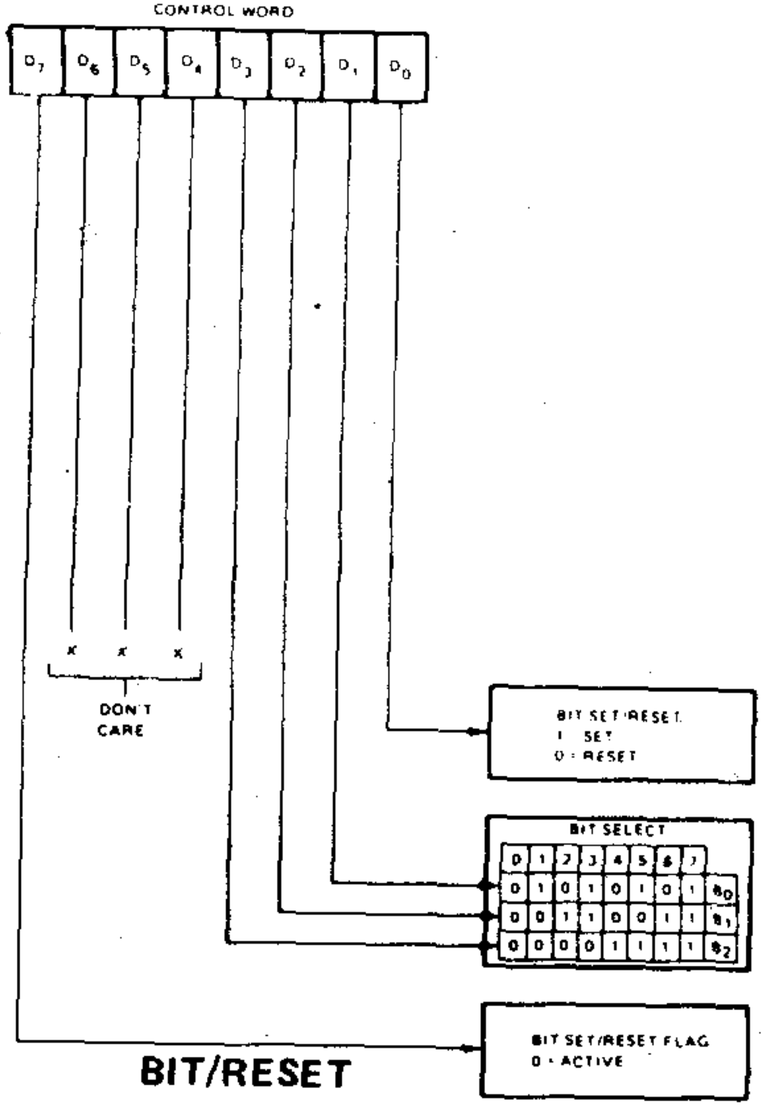
NOTES: ① X MEANS "DO NOT CARE"

② ALL CONDITIONS NOT LISTED ARE ILLEGAL AND SHOULD BE AVOIDED.

FORMATS



MODE DEFINITION



BIT/RESET